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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/678,375	10/03/2003	Kuei-Ann Wen	N0113/PP/HH	4031

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EXAMINER	
ROSSOSHEK, YELENA	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 12/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/678,375	WEN, KUEI-ANN	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the Application 10/678,375 filed 10/03/2003 and amendment filed 09/25/2006.

2. Claims 1-20 remain pending in the Application.

3. Applicant's arguments have been fully considered, they are partly persuasive.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Hakewell et al. (US Patent Application Publication 20050149898).

With respect to claim 1 Hakewell et al. teaches a modularized circuit design generating tool for designing working integrated circuit having a plurality of interconnected functional modules (paragraph [0012]), comprising a circuit module design database storing therein a plurality of pre-generated and commercially available circuit designs and corresponding specification information of functional modules of at

least two categories (within database 206 (paragraph [0076]) storing VHDL modules, wherein VHDL modules are predefined VHDL based designs (paragraph [0057]) and are selected by the user as specifically desired modules or functions for the circuit design (paragraph [0064])), wherein at least one category of the functional modules includes design information of circuit modules of at least two different specifications (within interactive architecture module for assembling the information about the designer's system, available libraries/specifications and the design configuration to be generated (paragraphs [0014]), [0064])); an element selection means allowing user to select suited circuit modules from the circuit module design database according to particular specifications of functional elements to be included into the integrated circuit to be designed (within an ability for the user to select specifically desired modules or functions for the design of the processor (paragraph [0064]) including gathering the information about the designer's system, available libraries and the design configuration to be generated (paragraph [0014])); a circuit module connection means to define connections between or among selected circuit modules according to features of each selected circuit module and thereby provides a circuit design of a working integrated circuit comprising the circuit modules (within a hierarchy generation module, which assists in ordering logical blocks or entities and routing signals within the design (paragraph [0014])); a memory to store circuit design information of the working integrated circuit and of all selected circuit modules and information of connections between and/or among the selected circuit modules (within an apparatus for implementation of the method of designing working integrated circuit/processor

including computer on the client site having internal and external storage device 3104 as depicted on the Fig. 31, wherein storage device is for storing the information downloaded from the server site using network (paragraph [0139])); and a file converting means to convert the circuit design information so obtained into an applicable format (within completing an VHDL file having all necessary information for integrated circuit design (paragraph [0136])).

With respect to claim 10 Hakewell et al. teaches a method for designing an integrated circuit having a plurality of functional circuit modules by using modularized circuit design information (within improved method for managing an integrated circuit design (paragraph [0013])) including limitations similar to the limitation of the claim 1.

With respect to claims 2-9, 11-20 Hakewell et al. teaches:

Claims 2 and 11: wherein the circuit module design information database comprises a communications tool connectable to a remote database within typical implementation of the database by residing on the server site using network environment with a client/server arrangements and integrated circuit design apparatus (paragraph [0139];

Claims 3 and 12: wherein the circuit design information database comprises a group of circuit design information files for central processing unit, a group of circuit design information files for processing element, a group of design information files for memory circuit and a group of circuit design information file for interfacing circuit (as shown on the Fig. 32 demonstrating developed integrated circuit using improved method for managing an integrated circuit design (paragraph [0013]), wherein circuit

comprises CPU, processor core, memory etc. (paragraph [0141]), and wherein the information for aforementioned components is stored in the database (paragraph [0076]));

Claims 4 and 13: wherein the group of circuit design information files for central processing unit comprises core circuit design information for at least two central processing units different in operational speed, length in instruction or bus width with each other (paragraph [0090]);

Claims 5 and 14: wherein the group of circuit design information files for processing circuit comprises circuit design information for at least two processing elements different in function (paragraph [0090]);

Claims 6 and 15: wherein the group of circuit design information files for processing circuit comprises circuit design information for at least one codec, at least one filter and at least one modulator (paragraph [0158]);

Claims 7 and 16: wherein the group of circuit design information files for memory circuit comprises circuit design information for at least two types of memory different in memory space (paragraphs [00150]-[0153]; [0181]);

Claims 8 and 17: wherein the group of circuit design information for interfacing circuit comprises circuit design information for at least two interfacing circuits different in function (paragraph [0143]);

Claims 9 and 18: wherein the group of circuit design information for interfacing circuit comprises circuit design information for at least one A/D converter, at least D/A converter, a USB interface circuit and a PCMCIA interface circuit (within variety of types

of the integrated circuit designs including different types of peripherals, such as A/D converters, D/A converters, interfaces, for example (paragraph [0142]));

Claim 19: a memory stored with circuit design information generated from the method of any of claims 10-18 within an apparatus for implementation of the method of designing working integrated circuit/processor including computer on the client site having internal and external storage device 3104 as depicted on the Fig. 31, wherein storage device is for storing the information downloaded from the server site using network (paragraph [0139]));

Claim 20: a circuit prepared with circuit design information generated from the method of any of claims 10-18 (paragraphs [0012]; [0057]).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helen Rossoshek
Examiner
Art Unit 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER